REMARKS

These remarks are responsive to the Office Action mailed June 5, 2007 ("Office Action").

ABSTRACT

In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

SPECIFICATION

Applicants submit this Substitute Specification (Attachment A) in response to the Office Action's objections (Office Action, pg. 5). Applicants respectfully submit that no new matter has been introduced in this substitute specification pursuant to 37 C.F.R. § 1.125(b).

Pursuant to 37 C.F.R. § 1.125(c), a marked-up copy of the Substitute Specification showing the changes to the specification is included as Attachment B.

STATUS OF THE CLAIMS

Claims 1-23 are currently pending in the present application, with claims 1 and 10 being the independent claims. Claims 1-16 are amended. Claims 17-23 are newly added claims.

35 USC § 103(a)

The Office Action rejects claims 1-16 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,515,826 to Hsiao et al. (Hsiao) in view U.S. Pat. No. 6,242,320 to So (So), and further in view of Hartmannsgruber, et al., "A Selective CMP Process for Stacked low-k'CVD Oxide Films", Microelectronic Engineering, Vol. 50, pg. 53-58, 2000 (Hartmannsgruber).

Newly amended claim 1 relates to a method for monitoring the process of thinning an active wafer provided as the one or two wafers of a bonded structure. The removal process, which comprises a CMP process, may be monitored and thus controlled by using a specific test

structure including a plurality of trenches of different width and thus of different depth. By assigning a target thickness of the active wafer to one of the trenches the advance in material removal during the complex removal process may be optically monitored, for instance by a successive exposure of trench corresponding to the target thickness of the active wafer.

In this respect, claim 1 explicitly refers to an optical detection of the exposure of the trenches, thereby providing for a simple yet highly reliable and robust technique for identifying an appropriate point of time for terminating the removal process.

After the reference trench corresponding to the target thickness is exposed, the active circuit may actually be formed in and/or above the active wafer, thereby enhancing the process uniformity and also the performance of the active circuit for many substrates, since the novel technique of the present invention provides for a significant reduction of substrate-to-substrate variation in thickness of the active wafer in SOI devices.

The concept of controlling a removal process for SOI substrates on the basis of a substrate internal test structure by optically detecting the exposure of trench corresponding to the target thickness is neither disclosed nor suggested by the prior art cited in the Office Action and also mentioned in the present application

So describes a process technique for enhancing surface topography in SOI substrates by forming isolation trenches with two different depths and filling the trenches with a CMP stop material. In a first CMP process the active wafer is thinned until the deeper stop trenches are exposed. Thereafter, a selective etch process is required to selectively recess the deeper trenches, while the shallow trenches are protected by the material of the active wafer. Hence, in this step a material removal of the active wafer is not obtained. Rather, an etch time controlled process may be required. Then, a further CMP process is performed in which the shallow trenches and the previously etched trenches are used as a CMP stop.

However, So does not describe a test structure comprising a plurality of trenches of different width varying in a systematic manner so that a clear optical indication is available for the progress of the removal process. Rather, So teaches employing two different CMP stop layers of different heights with an intermediate etch step for leveling the two CMP stop layers, thereby actually interrupting the material removal of the active layer of the wafer.

Hsiao describes the formation of induction coils in a dual layer structure. This document also describes a method for obtaining appropriate etch process parameters for forming an opening of the induction coil in a single etch process, while nevertheless arriving at two different

etch depths corresponding to the two different lateral dimensions of the induction coil opening, the windings and the contact portions. The etch parameters may be obtained on the basis of a test structure provided on a dedicated test substrate so as to identify a relationship between the lateral size, the etch time and the etch depth. Based on this finding, respective parameters may be used actual product substrates for forming the induction coil openings. however, this document does not disclose the usage of SOI substrates nor is in anyway suggested that the test structure for identifying appropriate etch parameters may be provided on actual product devices.

An optical detection of the exposure of trenches is also not referred to in this document

Thus, neither So nor Hsiao refer to a technique for enhancing substrate-to-substrate variations in SOI substrates on the basis of exposure of one or more trenches of different width and optical detection of the exposure. Furthermore, in particular, the test structure described by Hsiao is to be provided on a dedicated test substrate, since a plurality of test structures may typically be required so as to determine the dependency of etch time and etch depth of the individual trenches.

Moreover, although So relates to enhancing the surface planarity of SOI substrates during CMP, a completely different approach compared to the present invention is proposed, wherein even a combination with Hsiao, which there are no reasons to make, since Hsiao does not relate to enhancing uniformity of SOI substrates, could not provide technical advise as to how to further enhance substrate-to-substrate uniformity or process efficiency during the controlling of the material removal of the active wafer so as to obtain a superior semiconductor layer for the subsequent formation of the active circuits. For example, forming the CMP stop trenches in So with different widths would not be compatible with device requirements for trench isolation structures. Moreover, different widths and thus depths of trenches of So, when combined with Hsaio, would also not be compatible with reducing process complexity during the controlling of the CMP removal, since additional selective etch process would be required for adapting the various trench depth to the most shallow depth which would represent the target thickness of the finally obtained silicon layer thickness.

For at least these reasons, the teaching of claim 1 is non-obvious with respect to the alleged combination of So and Hsiao. In addition to these reasons, So and Hsiao, alone or in combination, do not teach or suggest an optical detection of the exposure of the trenches during a CMP process so as to identify a point in time corresponding to the desired thickness of the active wafer.

Similar arguments apply to claim 10, which now refers to an SOI structure including a test structure and active circuits, thereby allowing performing of the methods discussed above.

An indication of allowance of all claims is respectfully requested

CONCLUSION

Pursuant to 37 CFR § 1.136(a), Applicant hereby petitions for a Two-Month Extension of Time. Commissioner is hereby authorized to charge fees in the amount of $460.00 as set forth under 37 CFR § 1.136(a) for the Two-Month Extension of Time, to include responding up through November 5, 2007. In the event any variance exist, the Commissioner is hereby authorized to debit or credit undersigned's Deposit Account No. 50-0206 to cure any such underpayments or overpayments of fees as required.

A notice of allowance is earnestly solicited.

Respectfully submitted,

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Dated: November 2, 2007

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